REMARKS

Applicants have amended their claims in order to further clarify the definition of the present invention, and in order to facilitate proceedings in connection with the subject matter being claimed in the above-identified application. Specifically, withdrawn claims 14-21 and 27-30 are being cancelled without prejudice or disclaimer, and in particular without prejudice to the filing of a Divisional application directed to the subject matter thereof. In addition, claims 24, 25 and 31 are being cancelled without prejudice or disclaimer.

Furthermore, claim 32 is being amended to recite that the external connection terminals are provided only within the semiconductor device mounting region. Note, for example, Figs. 11f, 12f, 19e and 22g, of Applicants' original disclosure, together with, for example, descriptions on pages 30-32 and 41-56 of Applicants' specification. Note, also, for example, the description in the paragraph bridging pages 43 and 44 of Applicants' specification.

Initially, Applicants respectfully request that the present amendments be entered, notwithstanding finality of the Office Action mailed May 13, 2004. In this regard, it is respectfully submitted that especially in view of the canceling of various of the finally rejected claims, the present amendments materially limit issues remaining in connection with the above-identified application; and, at the very least, present the claims in better form for appeal. As will be discussed further infra, it is respectfully submitted that the present amendments, canceling withdrawn claims and various of the finally rejected claims, and further defining the present invention as set forth in claim 32, present all remaining claims in the application in condition for allowance. Moreover, it is respectfully submitted that the present amendments do

not raise any new issues, including any issue of new matter, by further clarifying the definition of the subject matter claimed in the present application. Note especially the previously referred to portions of Applicants' disclosure, as to why the present amendments do not raise any issue of new matter. In addition, noting the new grounds of rejection in the Office Action mailed May 13, 2004, including application of the newly cited U.S. Patent to Marrs, et al., and new arguments by the Examiner in connection therewith, it is respectfully submitted that the present amendments are clearly timely.

In view of all of the foregoing, it is respectfully submitted that Applicants have made the necessary showing under 37 CFR § 1.116(c); and that, accordingly, entry of the present amendments is clearly proper.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the prior art applied by the Examiner in rejecting claims in the Office Action mailed May 13, 2004, that is, the teachings of U.S. Patent No. 5,355,283 to Marrs, et al., and Japanese Patent Document No. 59-208756 (as designated by the Examiner, "Katsuhiko"), under the provisions of 35 USC §102 and 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a substrate for mounting semiconductor devices thereon as in the present claims, having, inter alia, the semiconductor device mounting region and a resin-sealing semiconductor package region outside of the semiconductor device mounting region, and wherein the external connection terminals of the plural sets of wirings of the substrate are provided only within the semiconductor device mounting region. See claim 32.

In addition, it is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a substrate for mounting semiconductor devices thereon as in the present claims, having, inter alia, plural sets of wirings which include a wire bonding terminal and an external connection terminal, and wherein the external connection terminal is provided only inside of the wire bonding terminal. See claim 33.

Furthermore, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested the other features of the present invention as set forth in the claims being considered on the merits in the above-identified application, having features as discussed previously in connection with claims 32 and 33, and further including (but not limited to) wherein the substrate includes a plurality of the semiconductor device mounting regions, with the plurality of regions respectively having blocks of wirings, each having a same pattern (note claim 32); and/or wherein the substrate includes a plurality of the wiring patterns comprised of a plurality of wirings arranged in rows and columns (see claim 34); and/or wherein the wire-bonding terminal includes a nickel layer and a gold plate layer on its surface (see claim 35); and/or wherein the external connection terminal is one of a plurality of external connection terminals, exposed on a surface of the insulating supporting member, on an opposite side to which the semiconductor device is mounted, the terminals being arranged in a grid pattern at positions corresponding to a device mounting region and a semiconductor package region of the substrate (see claim 36).

Moreover, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a semiconductor package as

in the present claims, produced by a method including use of the substrate according to claim 33 and mounting a semiconductor device on each of the plural semiconductor device mounting regions of this substrate, using a die-bonding material, with the semiconductor device being electrically connected by wire-bonding and the package region being sealed with a sealing resin connected in one piece; and with solder bumps being formed on the external connection terminals and wherein the substrate is cut so as to be separated into individual semiconductor packages. See claim 37.

According to the present invention, having location of the external connection terminals relative to the semiconductor device mounting region as in claim 32, and having a relative positioning of the external connection terminal and wire bonding terminal as in claim 33, package structure can be simplified and the package itself can be miniaturized to a greater extent. Moreover, according to the present invention wire bonding can be used with devices having reduced size, so that a large number of small-sized packages can be produced in a simple process, at a very low cost.

It is to be emphasized that the presently claimed structure, having positioning of, e.g., the semiconductor device mounting region and external connection terminals as in various of the present claims, has a "fan-in" structure for the external connection terminals, achieving greatly miniaturized package configurations with the external connection terminals, e.g., below the semiconductor device.

Marrs, et al. discloses a ball grid array in which one or more vias are formed through a substrate to electrically interconnect electrically conductive traces formed on a surface of the substrate to solder ball pads formed on another surface of the

substrate, the ball grid array including a substrate on which one or more integrated circuit chips (semiconductor dice on which electrically conductive circuitry is formed) are mounted, with passive components such as resistors and capacitors optionally also being mounted on the substrate. Bond wires connect bond pads on the integrated circuit chip or chips to electrically conductive traces formed on the surface (top surface) of the substrate to which the integrated circuit is mounted. Vias are formed in the substrate at locations at which it is desired to make electrical interconnection between traces on the top surface of the substrate and pads formed on the surface (bottom surface) of the substrate opposite the surface on which the integrated circuit chip is mounted; and electrically conductive material is deposited within the vias to electrically connect the traces and/or regions on substrate layers to traces and/or regions on other substrate layers or to pads on the bottom surface of the substrate. This patent to Marrs, et al. further discloses that the integrated circuit chip or chips and passive components are encapsulated with a resin by, for example, molding or potting, and that solder balls are formed on the pads on the bottom surface of the substrate. Note from column 2, line 60 to column 3, line 23. Note also column 3, lines 54-58; column 4, lines 8-13 and 42-60; and column 5, lines 49-68.

As can be seen, for example, in Figs. 2-6 of Marrs, et al., this patent discloses structure wherein the external terminals (for example, pads 208, 308, 408, 508 and 608 respectively in Figs. 2-6) fall outside the semiconductor device mounting region, and fall outside the wire bonding terminals (electrically conductive traces 205, 305, 405, 505 and 605 respectively in Figs. 2-6) constituting wire bonding terminals in Marrs, et al. It is respectfully submitted that Marrs, et al. would have neither taught nor would have suggested, and in fact would have taught away from, the presently

claimed subject matter including, inter alia, wherein the external connection terminals are provided only within the semiconductor device mounting region, as in claim 32; or wherein the external connection terminal is provided only inside of the wire bonding terminal, as in claim 33, and advantages thereof; as well as the other features of the present invention as discussed previously, and advantages thereof.

The contention by the Examiner in connection with previously considered claim 33, that Marrs, et al. in Fig. 2 shows an external connection terminal provided only inside of the wire bonding terminal, is respectfully traversed. As is clear in Fig. 2, the pad designated in Fig. 2 with reference character 208 falls outside the trace designated with reference character 205 in Fig. 2. Clearly, Marrs, et al. discloses external connection terminals outside of the wire bonding terminal, and would have taught away from such a substrate for mounting semiconductor devices thereon as in the present claims, wherein the external connection terminal is provided only inside of the wire bonding terminal.

It is respectfully submitted that the additional teachings of Katsuhiko would not have rectified the deficiencies of Marrs, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Katsuhiko discloses a semiconductor device package suitable for automated manufacturing, which provides heat radiation, wherein a semiconductor chip 15 (note Fig. 2D) is mounted 16 on a portion 11d and connected 19 to external electrodes 17, 18 on the portions 11h, 11i. This is all provided on Fe substrate 11. Transfer-molding with epoxy resin 20 is carried out, and the Fe substrate is removed by etching, to complete a leadless type package 21. Note the English Abstract of Katsuhiko.

As can be appreciated, for example, in Fig. 2D of Katsuhiko, et al., external electrodes 12b, 12c are provided directly under the wire bonding terminals. It is respectfully submitted that the combined teachings of Marrs, et al. and of Katsuhiko would have neither disclosed nor would have suggested such substrate for mounting semiconductor devices as in the present claims, including, inter alia, wherein the external connection terminals are provided only within the semiconductor device mounting region; and/or wherein the external connection terminal is provided only inside of the wire bonding terminal; and/or the other features of the present invention as discussed previously, and advantages achieved according to the present invention.

The Information Disclosure Statement submitted April 5, 2004, in the above-identified application, is noted. Submission of this Information Disclosure Statement on April 5, 2004, satisfied all applicable requirements of 37 CFR § 1.97 and § 1.98, such that the documents must be considered by the Examiner in the above-identified application. However, the Office Action mailed May 13, 2004, provides no indication that such documents were considered by the Examiner; that is, the Examiner has not provided Applicants with an initialed copy of the Form PTO/SB/08A submitted with this Information Disclosure Statement of April 5, 2004. Accordingly, it is respectfully requested that the Examiner indicate consideration of the documents submitted in the Information Disclosure Statement filed April 5, 2004, e.g., by providing Applicants with an initialed Form PTO/SB/08A. The Examiner is thanked in advance for complying with this request.

In view of the foregoing comments and amendments, entry of the present amendments, and reconsideration and allowance of all claims remaining in the application, are respectfully requested.

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Respectfully submitted,

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